SYNOPSYS®

DATASHEET

Platform Architect for Multi-Die

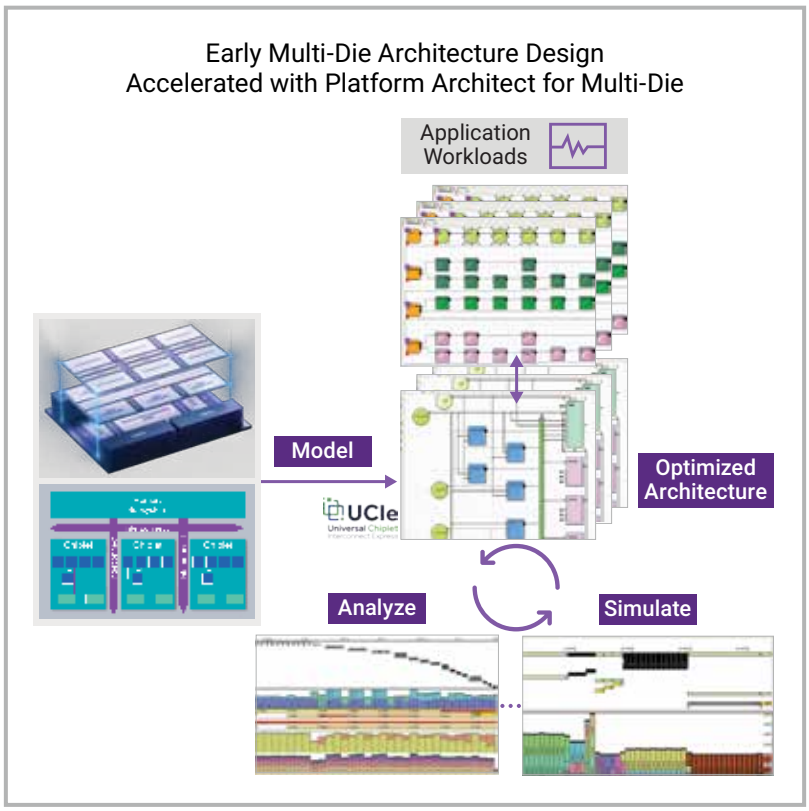
Early architecture exploration of multi-die designs

Overview

Synopsys Platform Architect for Multi-Die is a SystemC™ standards-based performance and power analysis tool for early architecture exploration of multi-die designs. It accounts for the interdependencies between multiple dies (also referred to as chiplets) within multi-die systems.

Platform Architect for Multi-Die helps optimize hardware-software partitioning, IP selection and configuration, interconnect and memory configuration, and power under consideration of the die-to-die interfaces. The solution includes a die-to-die model, including UCIe, as part of its library portfolio to compose a multi-die system for early architecture exploration.

Platform Architect for Multi-Die is part of the comprehensive Synopsys Multi-Die System Solution for accelerated heterogeneous integration and system disaggregation. The solution, including EDA and IP products, enables early architecture exploration, rapid software development and system validation, efficient die/package co-design, robust and secure die-to-die connectivity, and enhanced manufacturing and reliability.



Features

- Support for multi-die system architectures with die-to die models, including UCIe.
- Largest library of architecture models
- Fastest capture of task and trace-based SW workloads
- Application specific support (AI, automotive, networking, others)
- System-level power analysis based on IEEE-1801 UPF power monitors
- Intuitive analysis of tradeoffs and KPIs
- Fast design space sweeping and sensitivity analysis

Benefits

- Multi-die Support: Accounts for the interdependencies between multiple dies within multi-die systems
- Power Optimization: SoC interconnect and memory subsystem for performance and power optimization
- Partitioning & Optimization: Hardware-software partitioning, and IP selection and configuration
- Efficient Exploration: Traffic generation & cycle-accurate TLM interconnect models